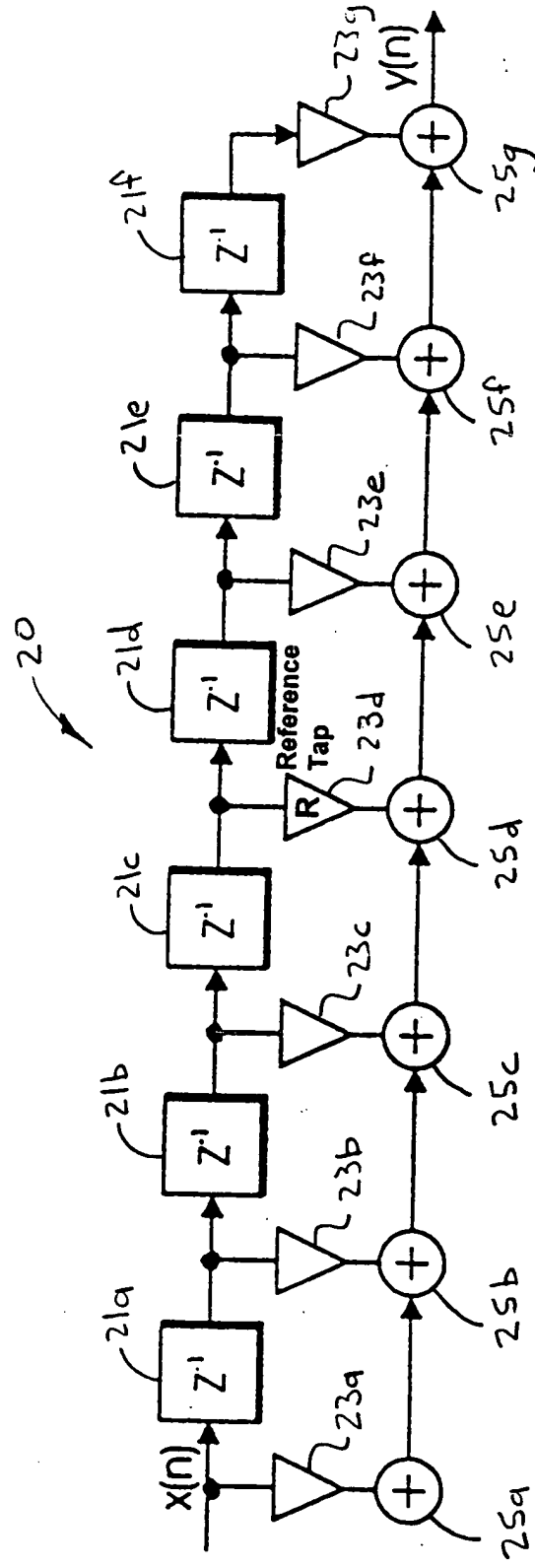
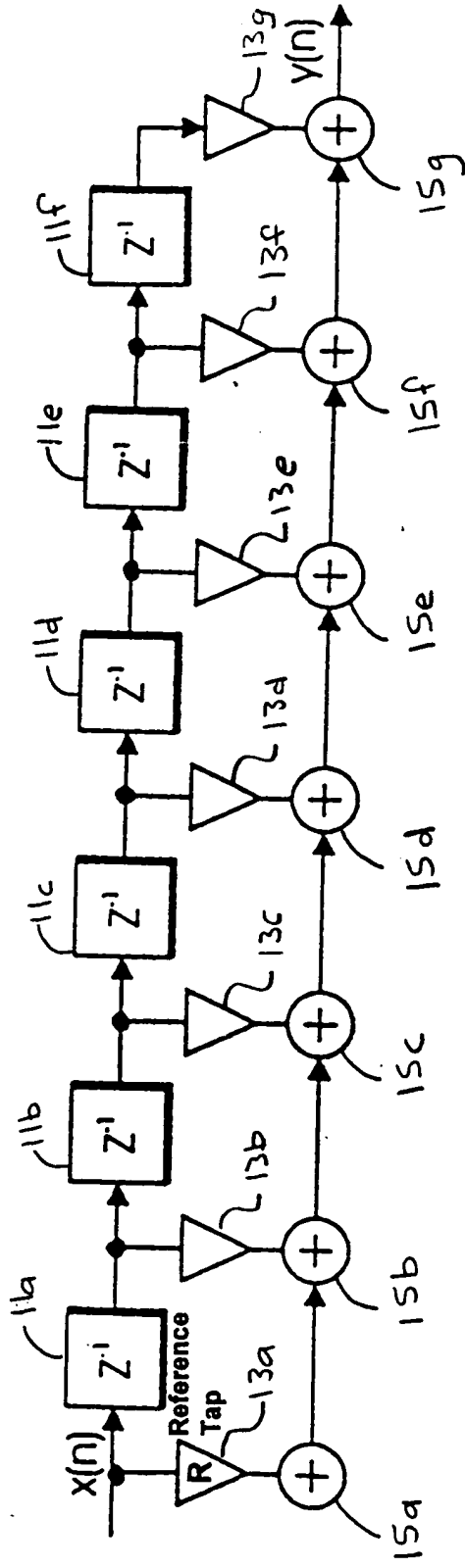
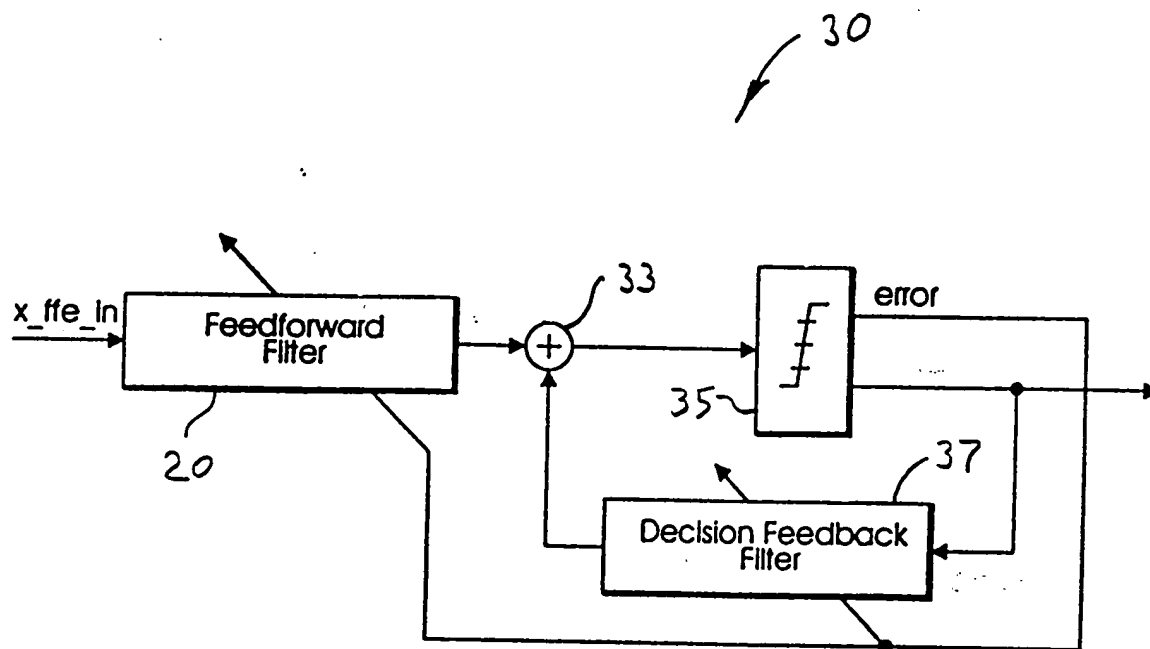


**FIG. 1**  
**Prior Art**



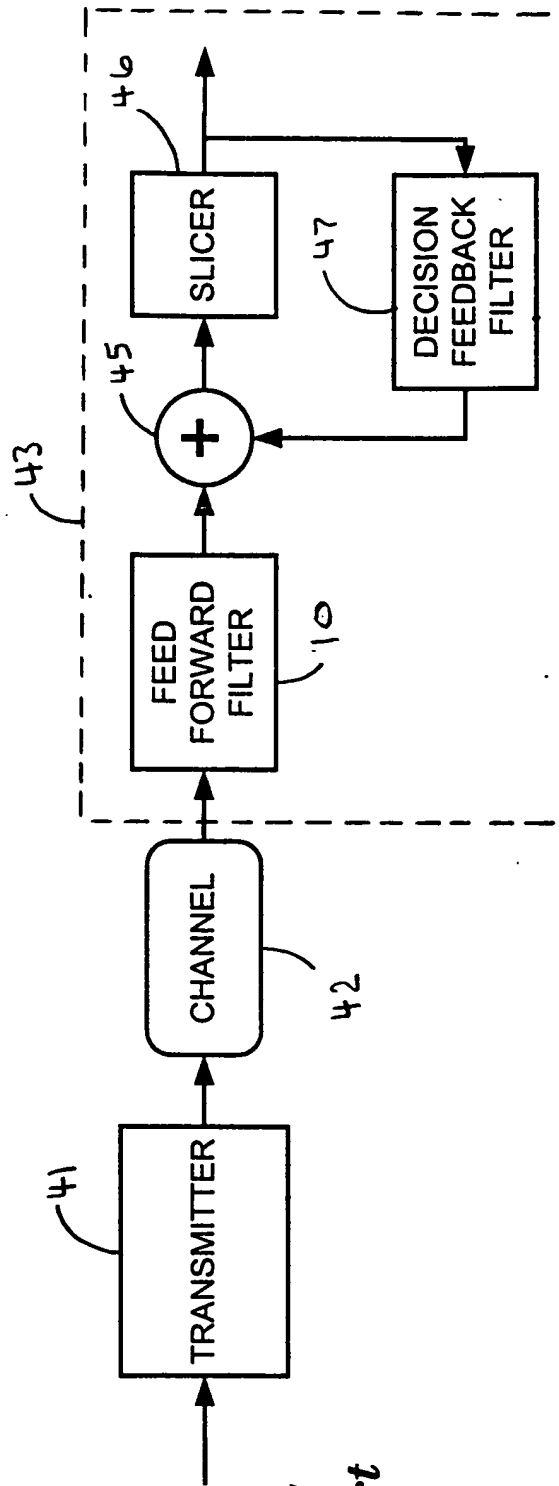
**FIG. 2**



**FIG. 3**

**FIG. 4**  
**Prior Art**

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FIG. 5

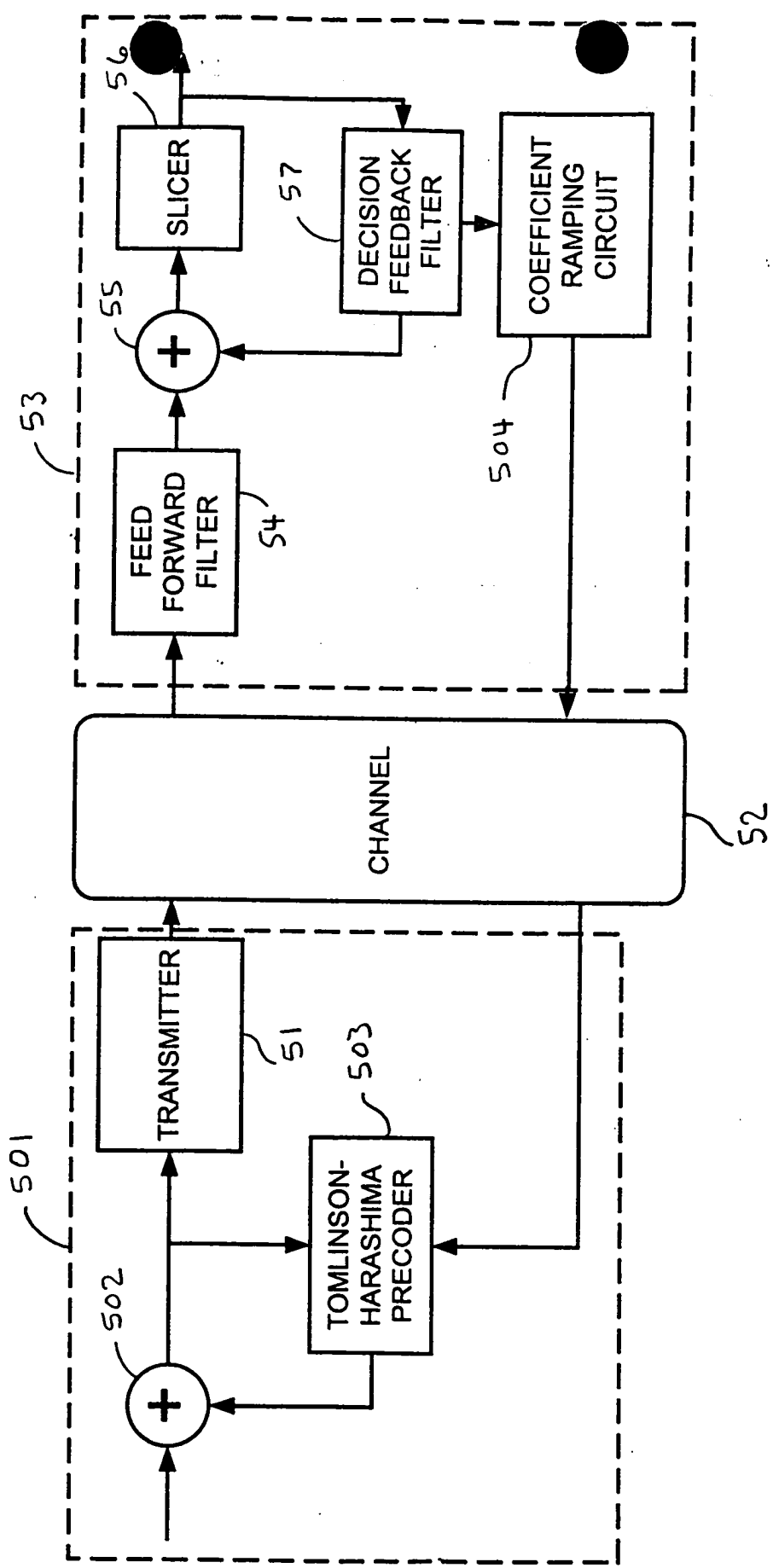
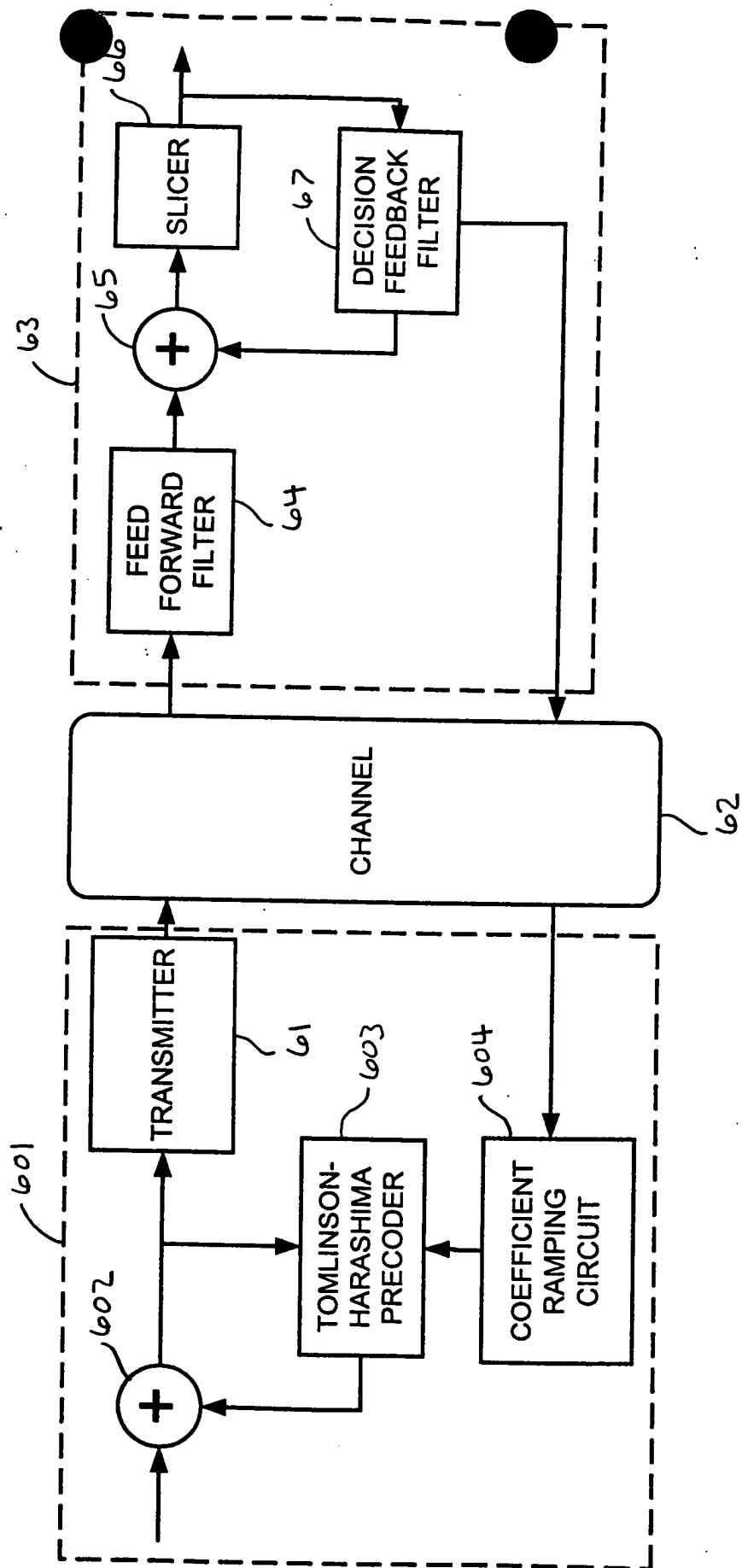
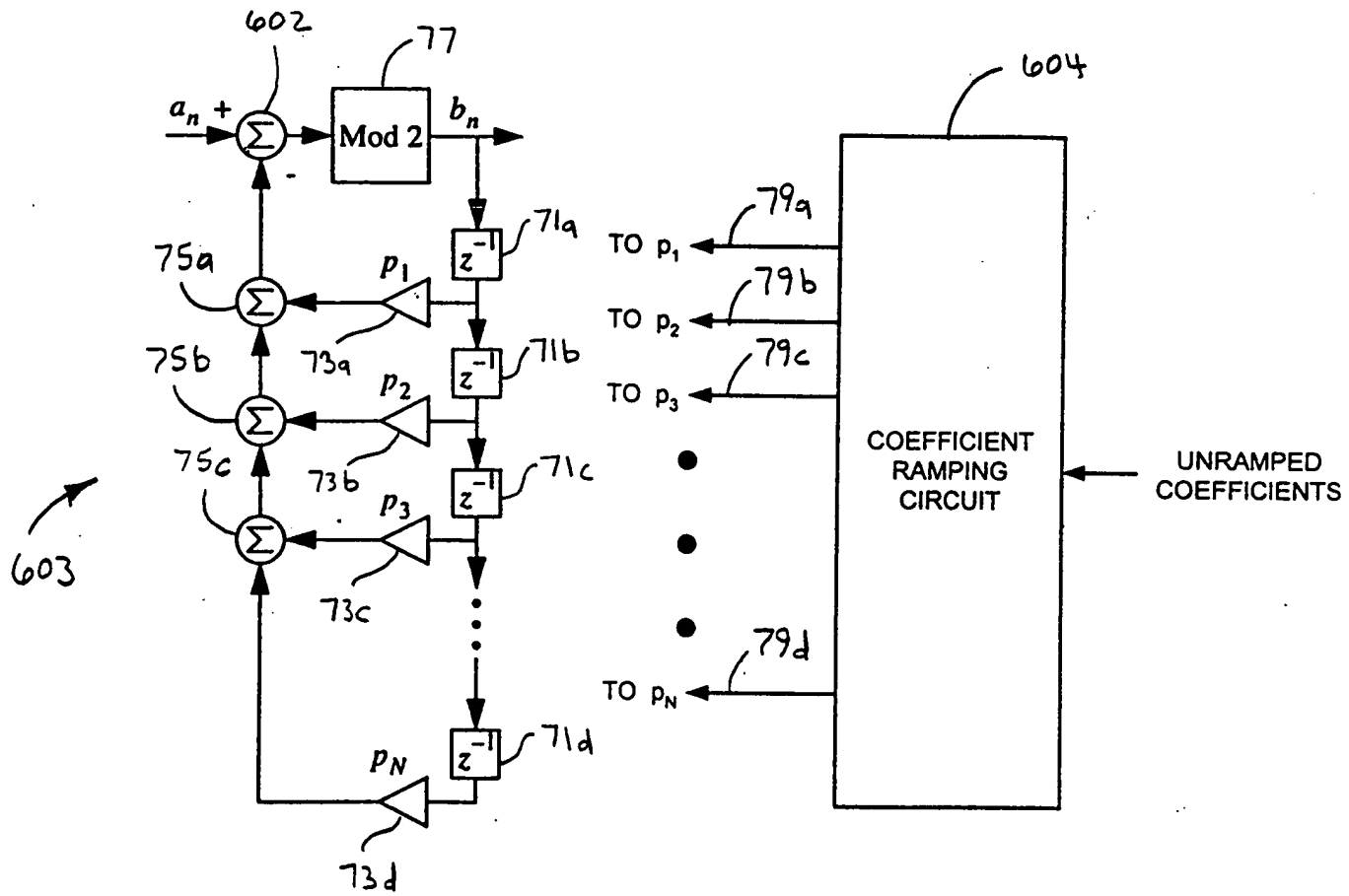


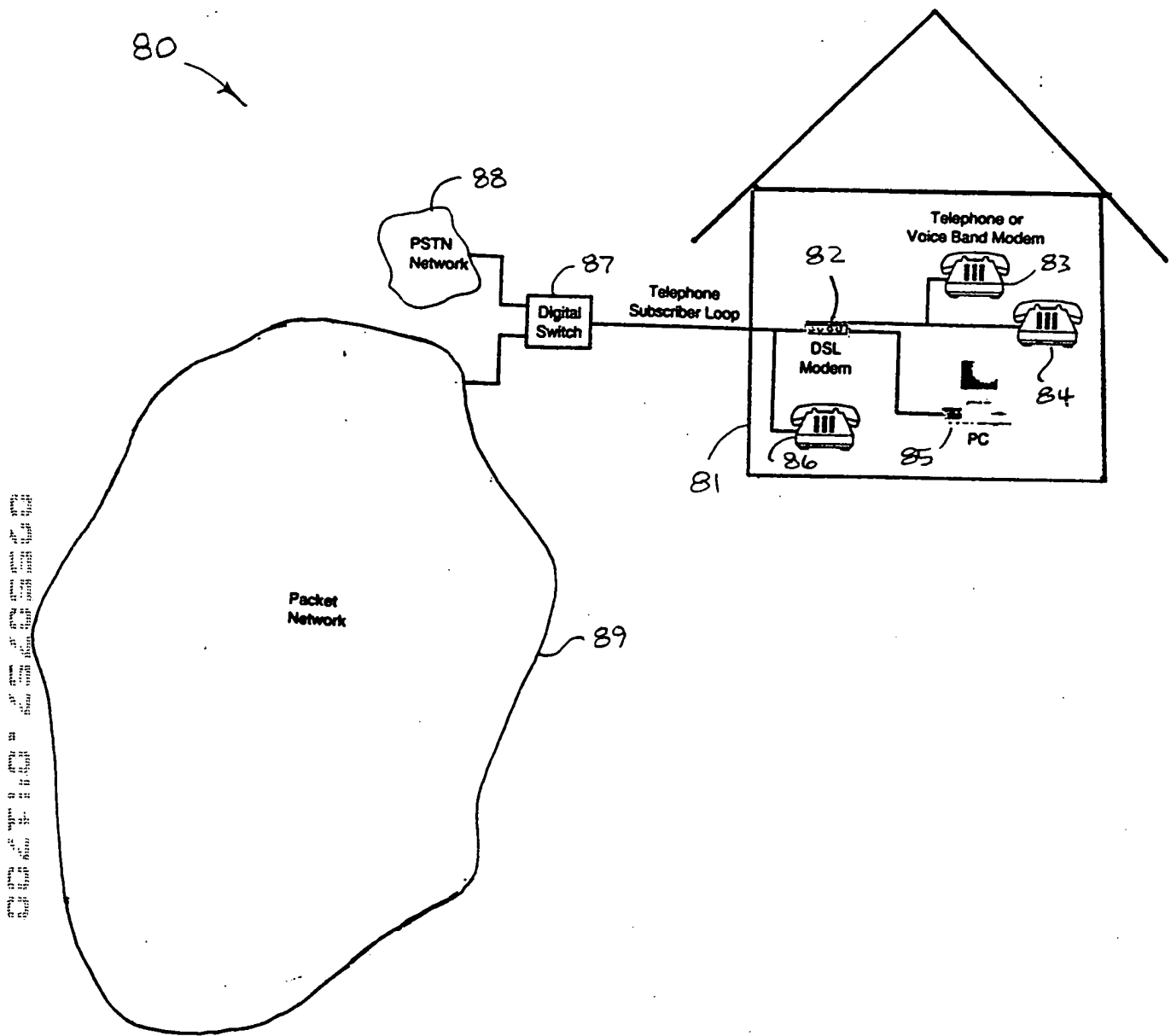
FIG. 6

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**FIG. 7**



**FIG. 8**

FIG. 9 is a block diagram of a digital communication system, such as a modem, which includes a transmit path and a receive path. The transmit path includes an error control coding block (91), a bit mapping block (92), a pre-coding block (93), a digital filter block (94), a DAC block (95), an analog filter block (96), and a POTS splitter block (907). The receive path includes a POTS splitter block (907), an analog filter block (98), an auto-gain block (99), a DAC block (901), an adaptive equalizer block (903), a symbol recovery block (904), an error de-coding block (905), and an echo canceller block (902). A coefficient training circuit (904) is connected to the pre-coding block (93) and the adaptive equalizer block (903). The system is connected to a twisted pair telephone loop and a POTS telephone set or voice band modem.

FIG. 9

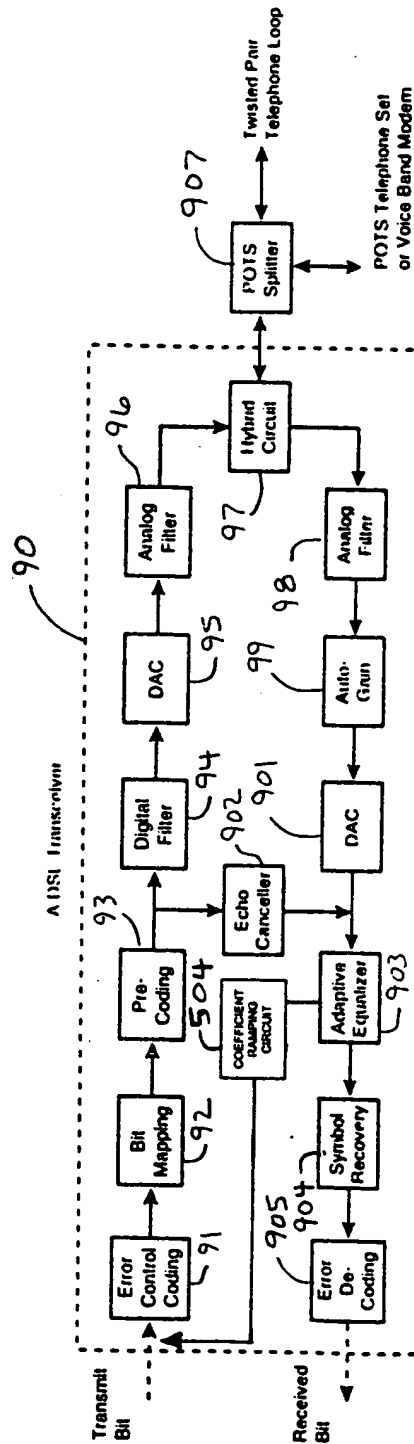




FIG. 10

